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DESIGN IMPLEMENTATION OF DIGITAL FM MODULATOR & DEMODULATOR FOR SDR USING FPGA

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ABSTRACT

This paper represents the recent advancement in the chip technology is integrating several sequential elements in System on Chip (SoC). But most of the circuits are using traditional clock distribution networks and facing the problem of skew and jitter problems. The clock signal generated by the oscillators and the flip-flops and registers are not receiving the clock pulse at the accurate time. The problem can be solved using Network of Phase-Locked Loop (PLL) oscillators coupled in phase. A phase locked loop ensures that the clock frequencies seen at the clock inputs of various registers and flip-flops match the frequency generated by the oscillator. The popular technique to demodulate FM signal is Phase Locked Loop (PLL). The existing technologies are based on software defined radio (SDR) [7, 8] and the demand needs programmable SDR instead of analog SDR. In SDR, Programmable digital devices are used and they transmit and receive the baseband signal at radio frequency. The recent cellular devices follow the communication protocol and provide connectivity to end user anywhere in the particular region.The design approach is based on digital components rather than analog components such as phase detector, loop filter and Voltage Controlled Oscillator (VCO). The signal is presented using digital words instead of analog voltages. In digital FM receiver, PLL is the main part to capture and lock the signals at different frequency and phase. The main purpose of PLL is to maintain the coherence between the modulated signal frequency (f_i) and the respective frequency (f_o), with the concept of phase comparison. PLL permits to track the frequency changes of applied input signals, as it is locked once. The paper focuses on the design, FPGA implementation of FM receiver integrated with digital PLL. There is a use of 8 bit analog to digital conversion (ADC) circuit, which is accepting frequency modulated signal as a series of digital numerical values. The same signals are demodulated by the receiver on every clock cycle. The paper proposed the design and FPGA implementation of digital PLL and programmable all FM receiver. The design is developed in Xilinx 14.2 ISE software and simulated in Modelsim 10.1b software with the help of VHDL programming language and the targeted onVirtex-5 FPGA.

KEYWORDS: System on Chip, Phase Locked Loop, SDR, VCO, FPGA.

I. INTRODUCTION

In a communication system [1] there are three modulation techniques, Amplitude Modulation (AM), Frequency Modulation (FM) and Phase Modulation (PM). In the ancient system all transmissions were analog. So the old PLL are based on analog blocks. Analog PLL have noise and gives diverse output. Digital PLL [4, 8] are based on digital clock signal and lock the signal with faster lock time. This is the necessity of rapid change of the technology present for our handset and base station used in 3G mobile scheme. The existing technologies are based on software defined radio (SDR) [7, 8] and the demand needs programmable SDR instead of analog SDR. In SDR, Programmable digital devices transmit and receive the baseband signal at radio frequency. The current cellular devices follow the communication protocol and offer connectivity to end user anywhere in the particular region. The technologies which are expending software and can process the data in real time use base on field programmable gate array (FPGA) or digital signal processors (DSP). Frequency modulation/demodulation is widely used schemes applied on mobile and FM devices. Audio and voice signal clearness is the main subject in mobiles. The signal generated in preserves a fixed phase relationship to a reference signal and it works in closed loop. . Current industries are fronting the problem of skew and jitter in clock and digital design. The problem can be resolved with the aid of designing an all-digital PLL that control the jitter involved in the function of PLLs to a higher degree that is disturbing the current communication industry.

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Phase Locked Loops (PLL) locks two signals in such a way that exist with same frequency and constant phase (zero) difference between them and is a closed loop system. The system matches the frequencies of an input waveform and output of PLL and then alters the frequency of output such that they are totally synchronized with each other. PLL consist of 3 parts: phase detector, loop filter and voltage controlled oscillator (VCO). The VCO helps in varying the output frequency and delivers frequency which is equal to the frequency of incoming signal. PLL locks two signals in a way such that they are matched. The incoming signal in the reference or input signal is the frequency that is to be adjusted so that it can match the reference signal and feed to VCO.

II. MATERIALS AND METHODS

Architectural Description

Phase Locked Loop (PLL) is the key part of SDR based FM demodulator. The PLL consist of three parts (i) Phase Detector (ii) Loop Filter (iii) Numerically Controlled Oscillator (NCO).The functional diagram of PLL is shown in Fig. 1. The purpose of the phase detector is to generate an error signal grounded on the difference in phase value between the input signal and the reference signal. The phase detector is a multiplier circuit producing additional signal. The output of multiplier is required to filter with the aid of a digital filter. The function of NCO is to generate a reference signal calculated by the error signal.

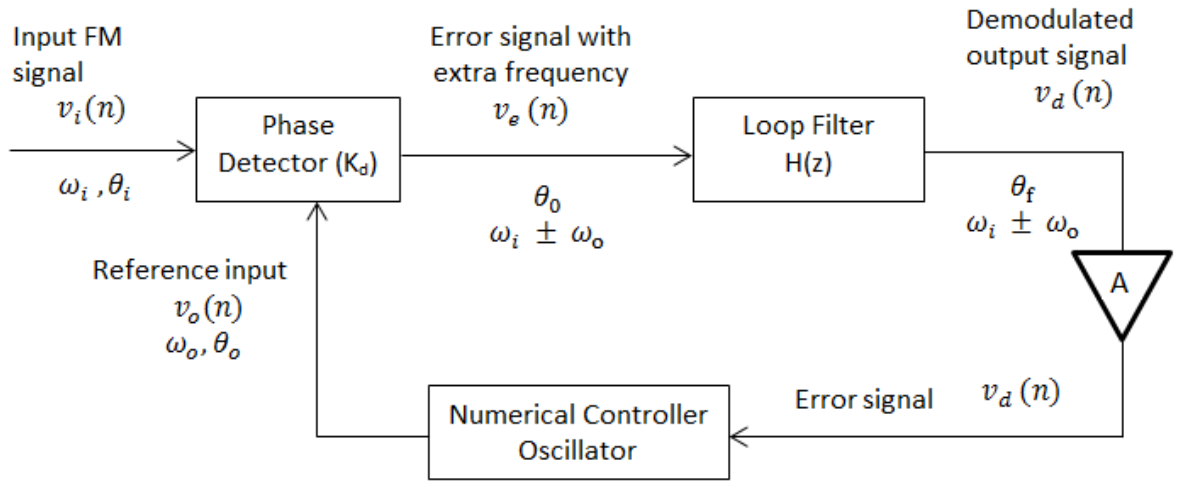

Fig. 1 Block diagram of PLL

PLL is most common module used in the System on Chip (SoC) processors and needed to provide clock pulse. PLL is used to generate a desired frequency for high precision crystal reference. The Frequency Synthesizer has the parameters frequency resolution, frequency range, switching speed, power and jitter consumption.

The block diagram of FM Receiver is shown in the Fig. 2. The key part of the FM is digital PLL. The function of PLL is to preserve coherence via phase comparison between the input modulated signal frequency (ω_i), and respective output frequency (ω_o). PLL certificates the tracking of frequency changes of the input signals with the self-correction capability of the system and lock the signal at specific frequency. The Frequency Modulated (FM) signal is measured as a series of numerical values or digital data .This is accomplished with the help of 8-bit Analog to Digital converter (ADC) circuit. FIR filter will provide the digital output and it can be transformed into FM. FM is a type of angle modulation system in which the instantaneous frequency of the carrier signal chamges linearly with the message signal m(t) as follows

$$S_{FM}(t) = A_c \cos\left[2\pi f_c t + 2\pi k_f \int_0^t m(n)dn\right] \qquad Equation\ (1)$$

Where A_c = Amplitude of carrier,
f_c = Frequency of carrier signal,
and K_f is frequency deviation constant.

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The FM receiver acquires the 8-bit modulated signal on every clock cycle and gives the demodulated signal output.

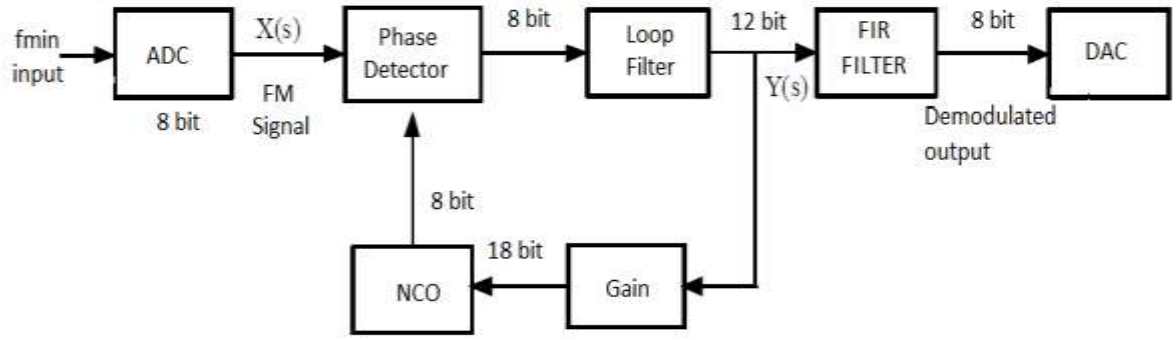

Fig. 2 Block diagram of SDR based FM receiver

Terms Related to PLL

- ***Lock range:*** The frequency range the PLL is able to remain locked. Mainly expalined by the VCO range.
- ***Capture range****:* The frequency range the PLL is capable to lock-in, starting from unlocked condition. This range is usually lesser than the lock range and will depend e.g. on phase detector.
- ***Loop bandwidth****:* Defines the speed of the control loop.
- ***Transient response*** Like settling time and overshoot and to certain accuracy (like 50ppm).
- ***Steady-state errors:*** remaining phase or timing error.
- ***Output spectrum purity:*** Like sidebands produced from a certain VCO tuning voltage ripple.
- ***Phase-noise:*** Given by noise energy in a certain frequency band (like 10 kHz offset from carrier). Largely dependent on VCO phase-noise, PLL bandwidth, etc.
- ***General parameters****:* power consumption, supply voltage range, output amplitude, etc.

System Design

The sketch of the system with various comments of FM is discussed sequentially and design aspects are also discussed.

Phase Detector

The purpose of the phase detector is to find the phase error between the input signal and the output signal coming from NCO. It is a multiplier circuit as shown in Fig. 3.

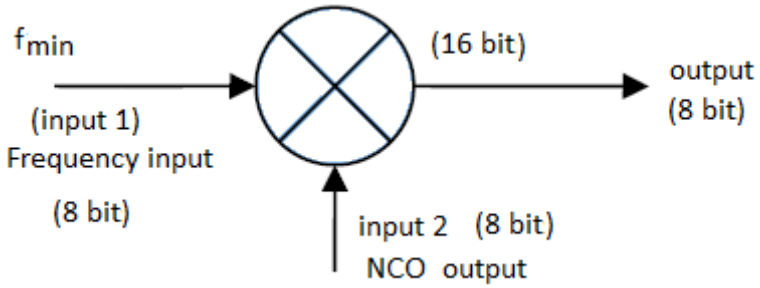

Fig. 3 Phase Detector

The signal provided to the phase detector is frequency modulated signal. Let the input signal to multiplier is $v_i(n)$ and given by equation 3.2.

$$v_i(n) = \sin(\omega_i n + \theta_i) \qquad Equation\ (2)$$

Where $\omega_i$input is signal radian frequency and θ_i is phase angle. The output of NCO is $v_o(n)$It is also sinusoidal and generated by NCO with feedback mechanism

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$$v_o(n) = \cos(\omega_i n + \theta_o) \qquad Equation\ (3)$$

The output of Phase detector to determine by the multiplication of the two signals

$$v_d(n) = k_d \sin(\omega_i n + \theta_i) \cos(\omega_i n + \theta_o)$$

$$v_d(n) = \frac{k_d}{2}[\sin(2\omega_i n + \theta_i + \theta_o) + \sin(\theta_i - \theta_o)] \qquad Equation\ (4)$$

Where K_d= gain of phase detector. Equation (4) is a combination of 2 terms. The term $sin(2\omega_i n + \theta_i + \theta_o)$ gives the high frequency components and second term $\sin(\theta_i - \theta_o)$ gives the phase difference in $v_i(n)$ and $v_o(n)$. The size of both inputs of the multiplier is 8-bit ,on multiplication the output is 16-bit. Input1 is minimum frequency input f_{min} and input2 is NCO output. On multiplication sealing is done so as to crop the most significant bits and the input of 8-bit is sent to the loop filter. There are many algorithms that can be used for multiplication like an array multiplier, Booth's multiplication. Booth multiplier gives optimised results in contrast to Array multiplier, so it is used in the design.

Loop Filter

The high frequency components given in Equation (3.4), are removed with the help of loop filter. Loop filter is a first order low pass filter. The transfer function of the loop filter is presented by Equation 3.5 and block diagram is shown in Fig. 3.4.

$$H(z) = \frac{1}{(z - \alpha)} \qquad Equation\ (5)$$

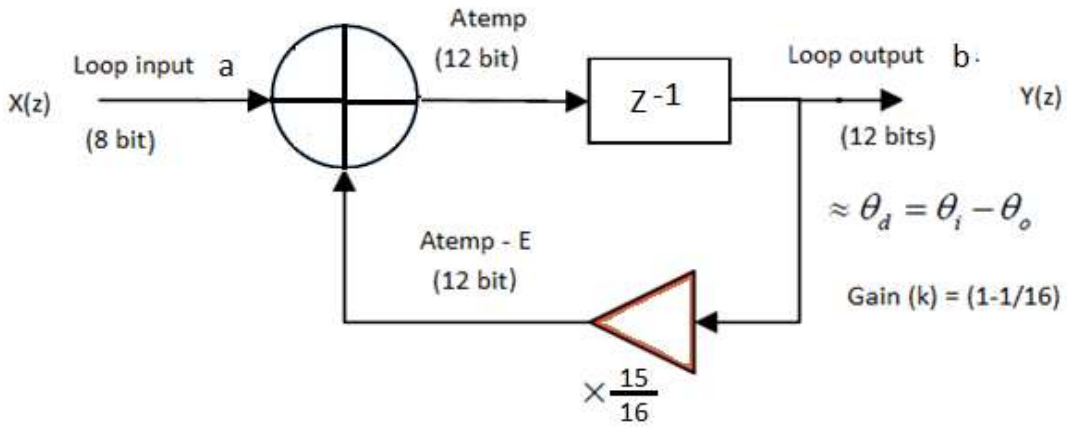

Fig. 4 Loop Filter

With the hardware implementation theme of view the above equation uses addition of the output signal from the register output and phase detector multiplied with a coefficient $\alpha = 1 - \frac{1}{16} = \frac{15}{16} = 0.09375$. The value of coefficient $\alpha = 0.09375$ lies within unit circle and ensures the stability of the system. The multiplication operation is done in such a way that extra multipliers are not required and multiplication can be done by just 4-bit right shift instead of a multiplier. The Equation (3.6) is written as

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1}{(z - \alpha)} = \frac{1}{(z - 0.09375)} \qquad Equation\ (6)$$

The input to the loop filter is *'a'* of 8-bit and out is b and is multiplied by 15/16 and then multiplication is sent back to 'a'. The sum of a and b is carried by d_{temp}(12-bits), an intermediate signal. d_{temp} is allocated, then

$$d_{temp} * \frac{15}{16} = d_{temp} * \left(1 - \frac{1}{16}\right) = d_{temp} - (d_{temp} * \frac{1}{16}) = d_{temp} - E$$

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The task $E = d_{temp} * \frac{1}{16}$is possible directly by shifting 4-bit right shift operation and no extra multipliers are obligatory.

Numerical Control Oscillator

NCO is also known as Direct Digital Synthesizer (DDS). The purpose of DDS is to take Corrective Error Voltage $v_d(n)$ and then shift its output frequency from its free running value to the incoming input signal frequency ω_i and thus keep the digital PLL in locking condition. The block diagram of NCO is shown in Fig. 5 and Fig. 6.

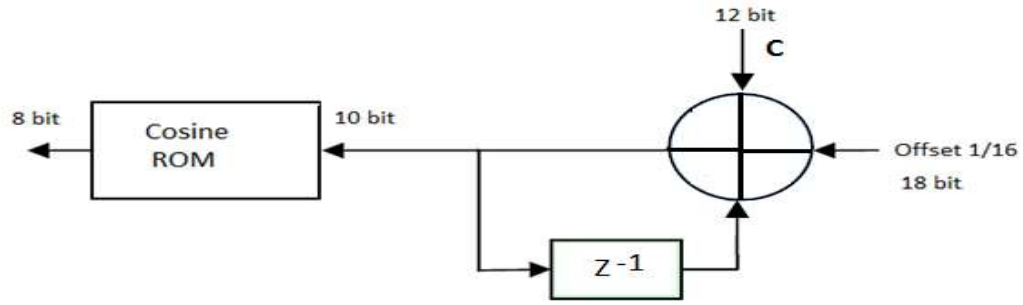

Fig. 5 Block diagram of NCO

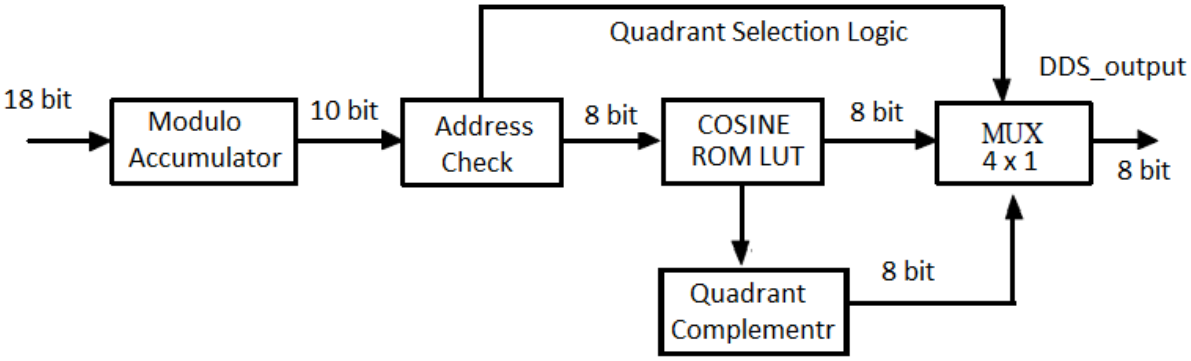

Fig. 6 Cosine ROM addressing

In the plan, let us assume that the free running frequency of NCO is 1 MHz and systems clock frequency is 16 MHz so, there are 16 sampling points in a cycle of free running frequency. In case of zero input, NCO produces an output equal to free running frequency. In hardware chip , Look up Table (LUT) technique is used to sample real values of sinusoidal input of 1 MHz A digital integrator circuit is taken to accumulate input values and kept in predefined locations of Cosine Rom. A Cosine signal is divided in 4 quadrants as shown in Fig. and 1 MHz frequency of DDS is well-defined using 1024 values of cosine signal. Grounded on 4 quarters distribution, first quarter has only 256 sample values. Hence, the ROM size of (256 x 8) bit is selected instead of (1024 x 8) bit to save the 1024 values of Cosine Rom. Other quarters in the Cosine ROM are duplicate of first quarter with a reverse sin of conversion to second and third. The depth of LUT and width is determined in such a way that it can withstand the minimum requirement for free dynamic range (SFDR) of 70dB. Accumulator is needed to accumulate the input phase and multiplexer for selecting the quadrant to assign the value is Cosine Rom based on LUT. The Rom address is of 10-bits. Input D_2 and offset value are summed and based on address mapping data values are saved in ROM locations.

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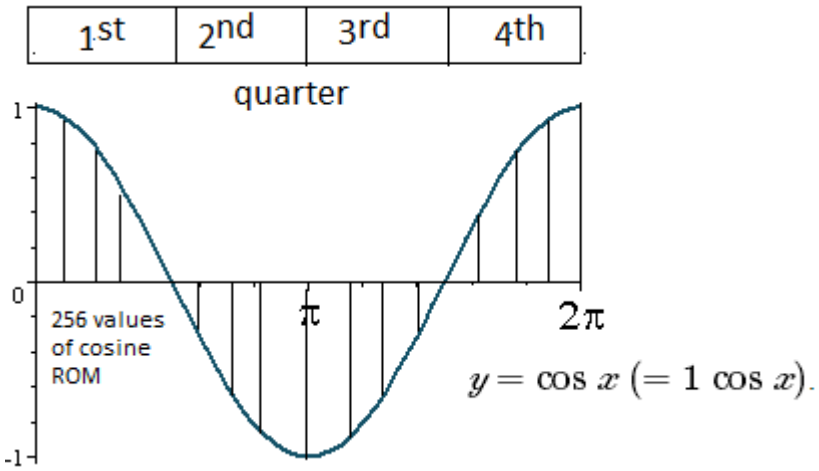

Fig. 7 Quarter wise values of one cycle of cosine ROM

The range of cosine ROM is collected data based on ROM address is given as
For first quadrant, $0 \leq i \leq 255$ - cosrom (i)
For second quadrant, $256 \leq i \leq 512$ - cosrom (512-i)
For third quadrant, $512 \leq i \leq 767$ - cosrom (i-512)
For fourth quadrant, $768 \leq i \leq 1023$ - cosrom (1024-i)

III. RESULTS AND DISCUSSION

RTL and Internal Schematics

The Register Transfer Level (RTL) view of the developed chip of FM demdulator is shown in Fig. 8 and function simulation in Modelsim software is shown in Fig. 9. This describes the pins used in the development of chip. The simulations are carried for the data by the chip. The simulation is done at a frequency of 98.00 MHz and received at the termination side or by the receiver.The snapshot is taken from the Modelsim 10.1 software. *CLK and Reset* are the inputs..

Step input1:*reset =1, clk* is used for synchronization and then run.
Step input 2:*reset =0, clk* is used for synchronization, force fmin and data_input and run

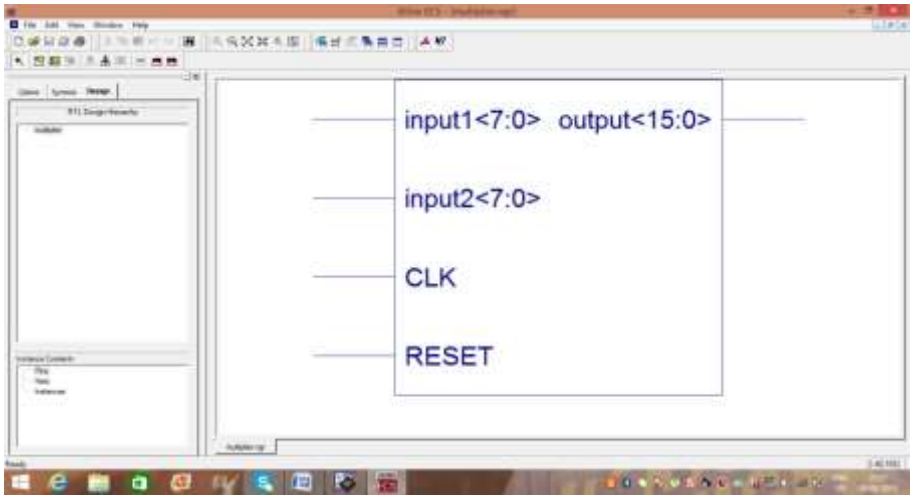

Fig. 8. RTL Output for phase detector

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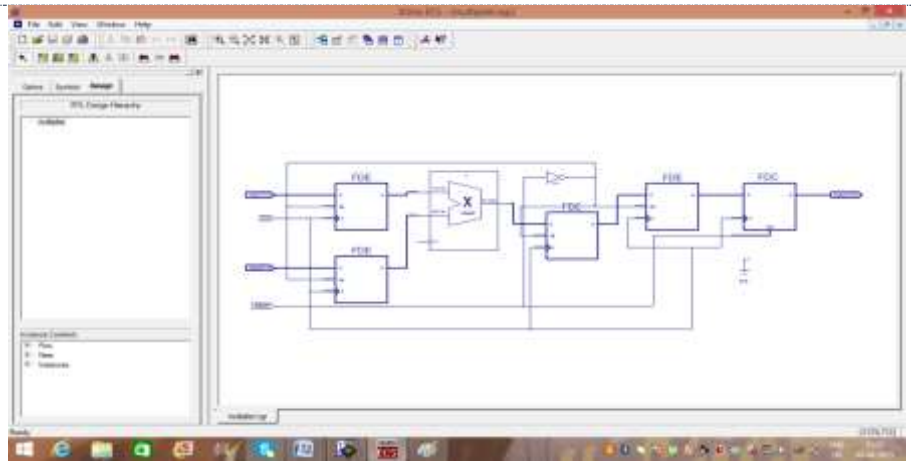

Fig. 9. Internal Diagram of phase detector

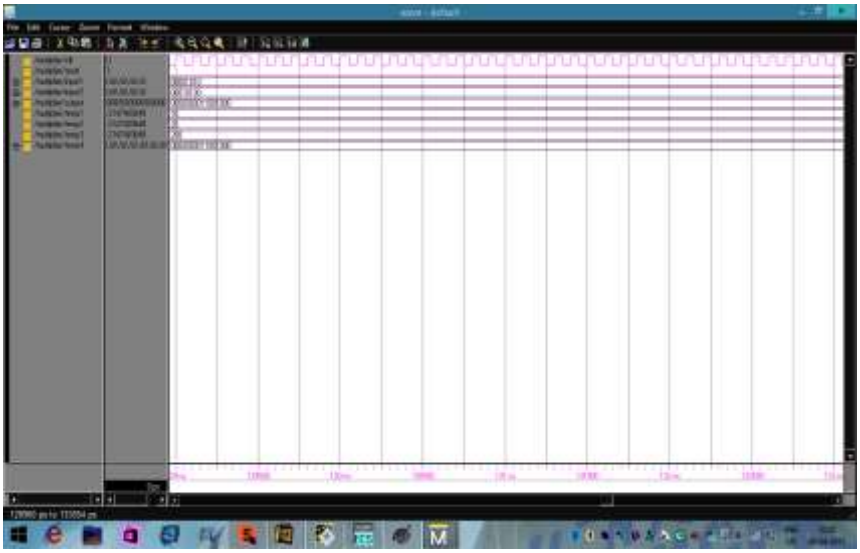

Fig. 10. Waveform Output of phase detector

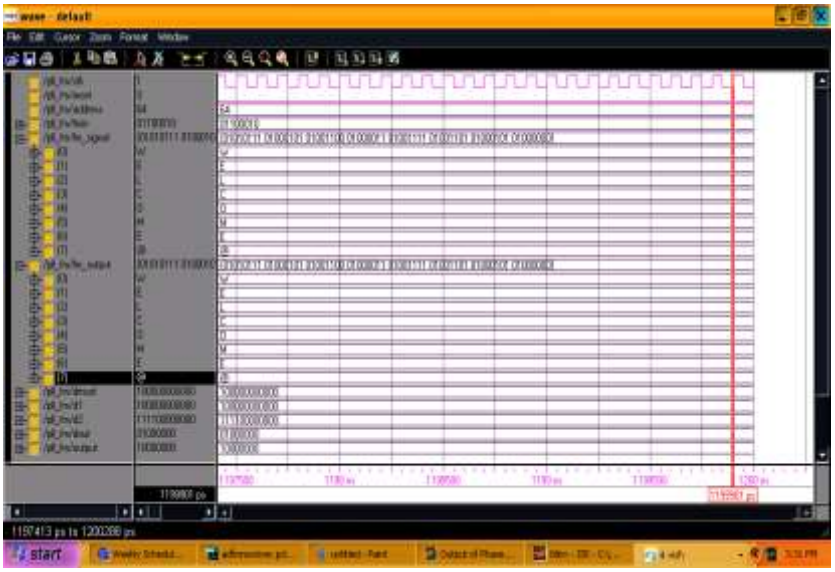

Fig. 11. Modelsim Simulation of programmable SDR

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IV. CONCLUSION

High performance software defined radio chip with varying frequency of 0-255 MHz is designed successfully. The code or clock synchronization is an important step in the decoding process. A digital phase locked loop can have many usages. If the data bits or clock bits are out of phase then the decoded bits can be decoded incorrectly. Also, if the decoder attempts to decode the bits away from the centre of the bits then minor variations could cause the decoder to decode the incorrect bit. The loop can also be used to synchronize to a repeatable code. This can be important if the dispreading code needed synchronized to the input.

The hardware simulation of the digital PLL chip with FM demodulator application is developed effectively using VHDL programming language in Xilinx 14.2 and simulated in Modelsim 10.1. The design is made on SPARTAAN-3E FPGA and verified on different test cases. The data is seen on the LCD on FPGA and Demodulated FM output is noticed on FM with the same frequency input given at input f_{min} of PLL block. The synthesis of the FM demodulator on SPARTAAN-3E FPGA is a newest work carried with optimized hardware, timing and memory optimization results. The work is overpowering the problems of existing analog PLL having problems like electrical noise, temperature variations and components aging etc. The design is programmable FM demodulator aptly suiting software defined radio. The design supports 13GBytes/sec of sustained memory bandwidth to the FPGA, 498 flip flops and low power consumption of 120mW. The developed design is an ideal solution for SDR-based next generation wireless communication transceiver circuit. We realize that it is good and easy to build, but needs high frequency of clock to drive the counters. Finally we try to implement our design into FPGA, and then we need to do real measurement. The result gives us the correct demodulated output wave as anticipated.

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